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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/658,597	09/11/2000	Steven P. Larky	0325.00418 CD117	4974

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CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/658,597	LARKY ET AL.	
	Examin r	Art Unit	
	Jeffrey R. West	2857	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 15 December 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ they raise the issue of new matter (see Note below);
   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____.
3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☐ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.
8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Continuation of 5:
Applicant first argues that "[p]age 3, line 16 thru page 4, line 3 of the Office Action appear to assert that it would have been obvious to combine Goutzoulis with Catalyst to cause a first USB between a personal computer and a host SBAE-10 device of Catalyst to operate at a first speed and a second USB between the host SBAE-10 device and an exercised SBAE-10 of Catalyst to operate at a second speed faster than the first speed. However, the Office Action fails to state if the modification slows the first speed for the first USB and/or increases the second speed for the second USB." Applicant then provides arguments regarding the motivation to combine if the proposed modification slows the first speed and argues the expectation of success if the proposed modification increases the second speed.
The Examiner asserts that page 3, line 16 to page 4, line 3 of the final Office Action does not suggest the inclusion of any further USB devices. This section of the Office indicates that the invention of Catalyst describes performing an automatic adjustment to test the device at an appropriate speed but is silent on how this adjustment is performed. Goutzoulis is then included to teach a method for providing such an adjustment by transferring low-speed vectors to a test device which generates high-speed test vectors (i.e. vectors at a second speed faster than said first speed) for transfer to a digital DUT (column 2, lines 50-54 and column 2, line 60 to column 3, line 7 column 2, lines 50-54).
Therefore, since the proposed modification does not require the addition of further complexity, Applicant's arguments regarding this feature are moot.

Applicant then argues that "[c]laim 1 further provides the host emulator having (ii) a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device. In contract, Goutzoulis appears to teach that the conversion from a low-speed parallel signal to a high-speed serial signal produces a unidirectional interface. In particular, an optoelectric converter 26 used by Goutzoulis to present the high-speed signal in electrical form to the DUT 28 does not appear to be capable of receiving an electronic signal back from the DUT 28. Therefore, Catalyst and Goutzoulis, alone or in combination, do not appear to teach or suggest a host emulator having (ii) a second interface configured to (a) transmit a test vector to a device and (b) receive a response from the device as presently claimed."
The Examiner asserts that the invention of Goutzoulis is only used to modify the invention of Catalyst to include a method for performing the high-speed adjustment. The invention of Catalyst teaches the main configuration and operation of the invention and does include a bi-directional interface that transmits a test vector to a device and receives a response from the device (User's Manual, page 6, Figure 3).

Applicant also argues that "[c]laim 7 further provides a test vector generator configured to generate a test vector. In contrast, Goutzoulis appears to be silent regarding a test vector generator for generating the data stored in the memory 10. Catalyst appears to allocate test vector generation to a user and/or PC (asserted to be similar to the claimed low speed tester but not the claimed test vector generator). Therefore, Catalyst and Goutzoulis, alone or in combination do not appear to teach or suggest a test vector generator (independent of a low speed tester) configured to generate a test vector as presently claimed."
The Examiner asserts that the invention of Goutzoulis teaches a circuit that reads out test vectors from the memory according to a clock signal (column 2, lines 60-63) and therefore must inherently include some type of test vector generator for loading the test vectors into the memory. Goutzoulis also teaches, in a preferred embodiment, that the test vector generator is a software that generates the test vectors and stores them in the memory (column 1, lines 34-36).

Applicant then argues that "[c]laim 7 further provides (from claim 4) that the test vector generator transfers the test vector to a low speed tester. Assuming, arguendo, that Goutzoulis somehow teaches a test vector generator . . . Goutzoulis does not appear to present the test data stored in the memory in a format suitable for a low speed tester. In particular, FIGS. 1 and 3 of Goutzoulis appear to transfer the test data directly to the DUT 28 at high-speed. Even if the test data were routed to a low speed tester, no reasonable expectation of success appears to exist for the low speed tester to properly receive the high speed test data."
The Examiner maintains that the test vector generator of Goutzoulis produces data for storage in a memory. These test vectors are not high-speed and are a suitable form for a low-speed tester, and therefore the combination is proper.

Applicant then argues that "[c]laim 13 further provides a low speed tester configured to generate a pass/fail signal. In contrast, page 5, lines 12-14 of the Office Action state that Catalyst provides a pass/fail signal . . . [p]age 2 of the User's Manual indicates that the host SBAE-10 device may generate a pass/fail signal for a current inrush test. However, the Office Action appears to consider the host SBAE-10 device to be similar to the claimed host emulator. Thus, Catalyst appears to allocate generation of a pass/fail signal to the wrong claim element."
The Examiner maintains that the invention of Catalyst teaches generating pass/fail data (i.e. signals) at the host device for transfer to the PC (i.e. low speed tester) that then uses the data to generate a pass/fail signal suitable for display to a user through a GUI.
Applicants argument that the assertion "that a user may decide pass or fail from the data displayed on the PC is moot since a user is not part of the circuit" does not convince the Examiner that a "pass/fail signal" cannot be broadly interpreted as test data that indicates whether the device passes or fails